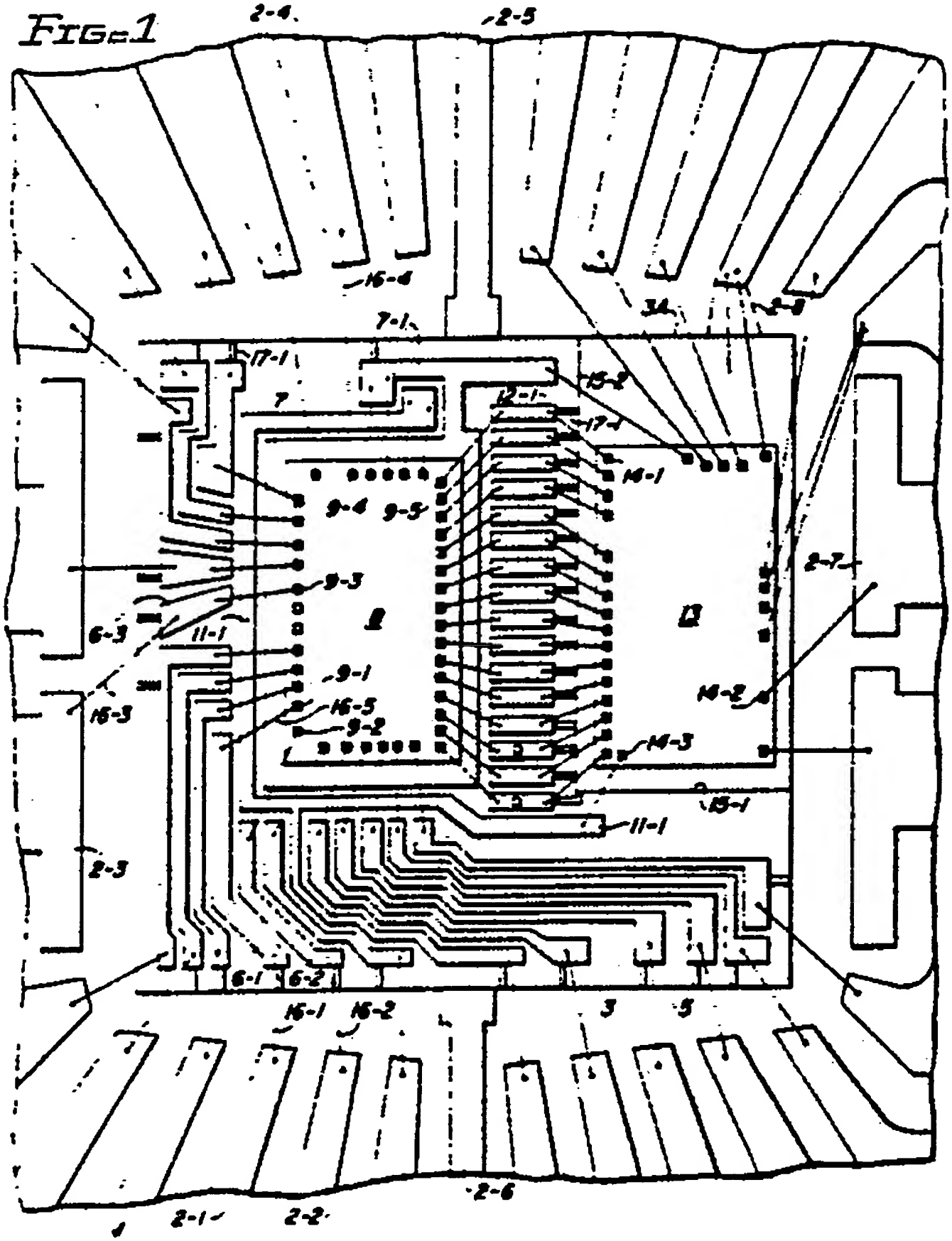
No English title available.

Patent Number: DE3916980
Publication date: 1989-12-14
Inventor(s): HOBSON LARRY D (US)
Applicant(s): BURR BROWN CORP (US)
Requested Patent: KR9705724
Application Number: DE19893916980 19890524
Priority Number(s): US19880201589 19880602
IPC Classification: H01L21/56; H01L25/16
EC Classification: H01L23/495C8, H01L23/495L
Equivalents: FR2632454, GB2219435, JP1977757C, JP2032558, JP7012071B

Abstract

A hybrid circuit includes an insulative film (5) bonded to a first area of a die attach pad, a second area (3A) of the die attach pad being exposed. A plurality of individual metalized strips (6, 11, 12) and a first die attach area (7) are formed on the film. A first integrated circuit die, (8), such as a low power MOS chip, is bonded to the first die attach area, and a second integrated circuit die (13), such as a high power bipolar chip, is bonded to the second area of the die attach pad. Bonding wires (16) are bonded to connect various bonding pads (9, 14) of the two integrated circuit dice to various metalized strips (6, 11, 12) on the insulative film and to lead frame fingers (2). The dice, bonding wires, die attach pad, lead frame fingers, and insulative film are encapsulated in plastics by transfer molding.

FIG-1


2-4
2-5
16-4
7-1
17-1
7
12-1
15-2
17-2
14-1
9-4
9-5
9-3
11-1
9-1
16-5
9-2
16-3
6-3
2-3
2-7
14-2
14-3
15-1
11-1
6-1
6-2
16-1
16-2
3
5
2-6
2-1
2-2

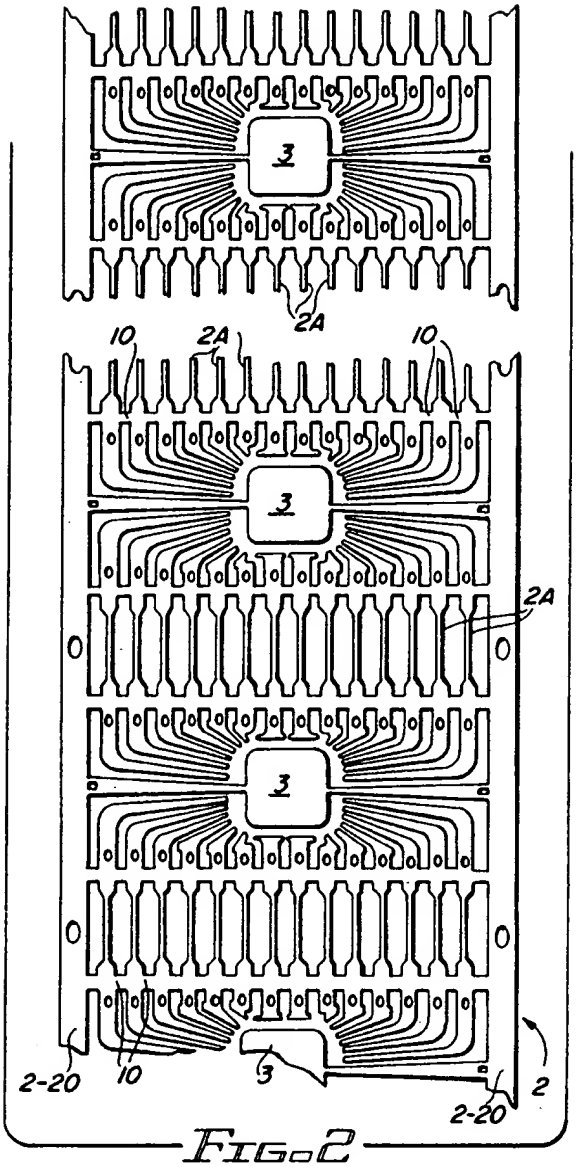


FIG. 2

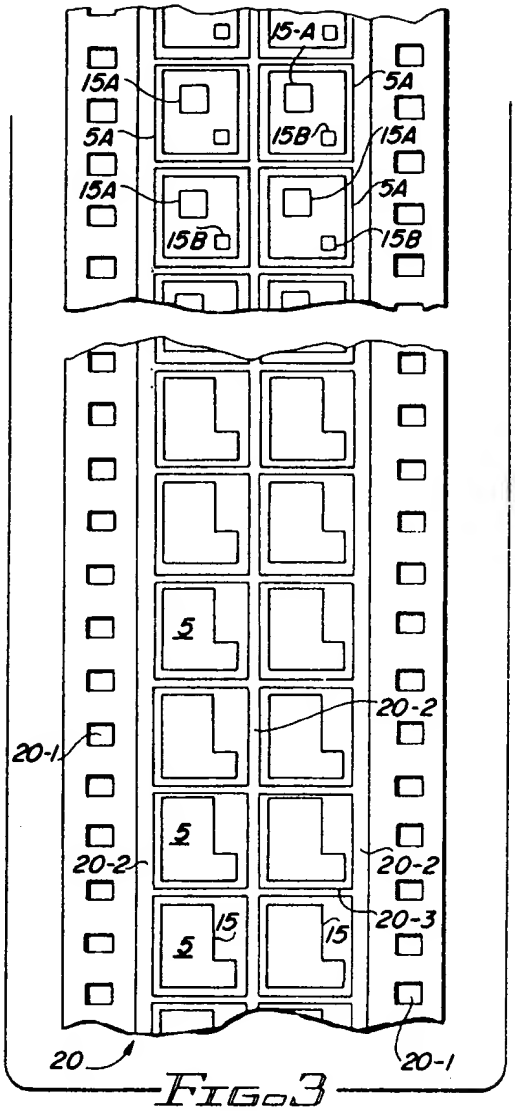


FIG. 3

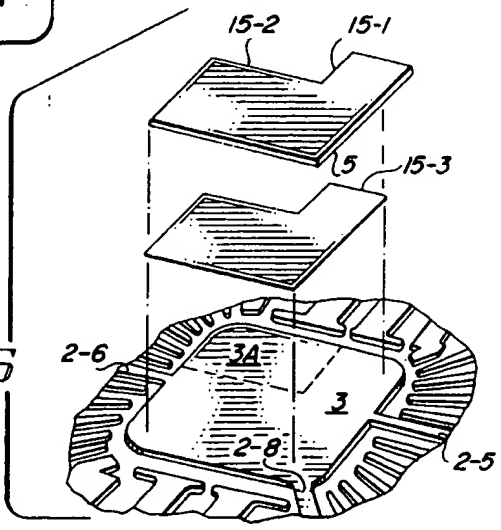


FIG. 5